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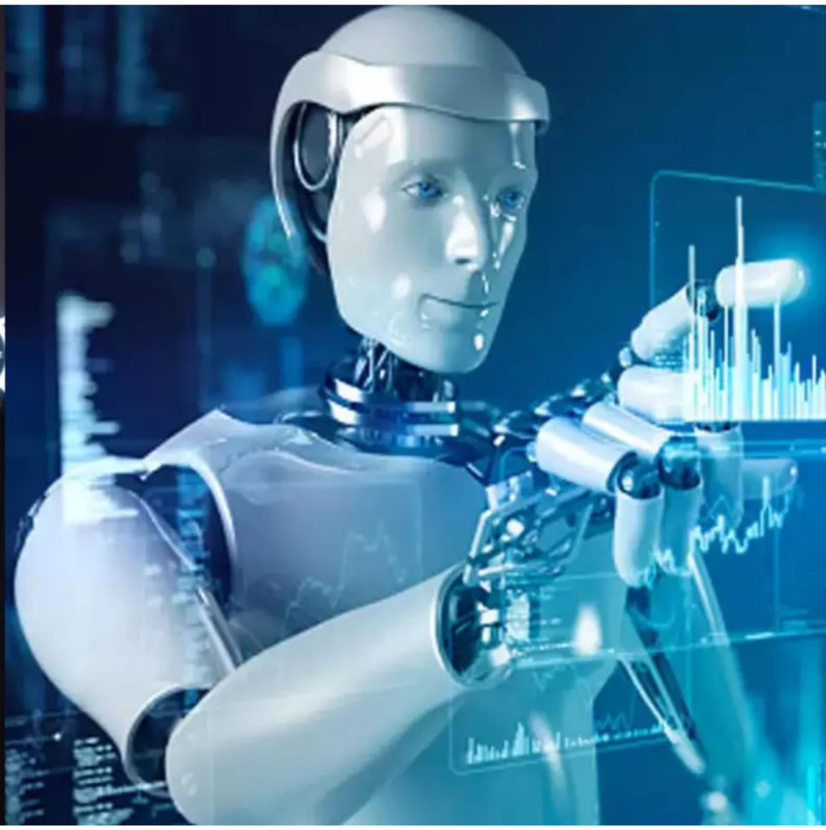

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Design, Timing Analysis and Power Optimisation of CMOS Digital Circuits in UMC 65nm Technology

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ABSTRACT: This paper presents the design, simulation, and timing analysis of fundamental CMOS digital circuits implemented in UMC 65nm technology using Cadence Virtuoso. Three core circuits are designed and analysed: a CMOS inverter, a tri-state inverter, and an edge-triggered D flip-flop. Each circuit is evaluated at both schematic and post-layout levels following parasitic extraction (PEX). Fan-out analysis from FO1 to FO8 is performed to validate logical effort theory, and a long-wire experiment quantifies the impact of interconnect geometry on propagation delay. Supply voltage scaling from 0.6 V to 2.0 V reveals the delay-energy trade-off, with a minimum energy point identified near 0.8 V. The measured inverter propagation delay of approximately 32 ps at 1 V supply is consistent with theoretical RC delay models. Results confirm that layout-aware design and parasitic extraction are essential for accurate performance prediction in nanoscale CMOS technologies.

KEYWORDS: CMOS, UMC 65nm, propagation delay, fan-out, logical effort, parasitic extraction, tri-state inverter, D flip-flop, minimum energy point, Cadence Virtuoso.

I. INTRODUCTION

The continuous scaling of CMOS technology into the deep submicron regime has enabled high-performance, low-power integrated circuits. At the 65 nm technology node, circuit behaviour is increasingly dominated by interconnect parasitics and short-channel effects such as velocity saturation, threshold voltage roll-off, and drain-induced barrier lowering (DIBL). These phenomena directly influence switching delay, noise margins, and overall circuit reliability [7].

Basic logic cells — inverters, buffers, and flip-flops — form the fundamental building blocks of all digital systems. While conceptually simple, their physical implementation in nanoscale technologies introduces non-ideal parameters that significantly affect timing performance. Interconnect resistance introduces delay, metal routing increases load capacitance, and fan-out loading alters switching behaviour. Consequently, parasitic extraction becomes essential for accurate delay estimation.

This paper presents the complete design and timing analysis of three fundamental CMOS circuits in UMC 65 nm technology: a CMOS inverter, a tri-state inverter, and an edge-triggered D flip-flop. Fan-out analysis, wire delay characterisation, supply voltage scaling, and minimum energy point identification are also performed.

II. THEORETICAL BACKGROUND

A. CMOS Operation and Propagation Delay

A CMOS gate consists of a complementary pull-up network (PUN) using PMOS devices and a pull-down network (PDN) using NMOS devices. The first-order RC delay model approximates propagation delay as:

$$t\_pd \approx 0.69 \times R\_eq \times C\_L \quad ...(1)$$

where R_eq is the effective on-resistance and C_L is the total load capacitance:

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$$C\_L = C\_gate + C\_diffusion + C\_wire \quad ...(2)$$

Average propagation delay is expressed as:

$$t\_pd = (t\_PLH + t\_PHL) / 2 \quad ...(3)$$

B. Fan-Out and Logical Effort

From logical effort theory, the normalised delay of a gate is:

$d = g \cdot h + p \quad ...(4)$

where g is the logical effort, h is the electrical effort (fan-out), and p is the parasitic delay. Since p remains constant, total delay does not scale linearly with load.

C. Wire Delay

A lumped RC approximation for wire delay is:

$t\_wire \approx 0.38 \times R\_wire \times C\_wire \quad ...(5)$

As metal dimensions shrink, wire resistance increases while capacitance scales more gradually, making layout-aware timing analysis essential.

III. CMOS INVERTER DESIGN AND ANALYSIS

A. Schematic Design and Device Sizing

The CMOS inverter was implemented in UMC 65 nm technology using P_12_LLRVT PMOS and N_12_LLRVT NMOS devices at 1 V supply. The selected transistor dimensions were PMOS: W = 560 nm, L = 60 nm and NMOS: W = 350 nm, L = 60 nm. The width ratio Wp/Wn ≈ 1.6 compensates for the lower hole mobility in PMOS devices, targeting near-symmetric rise and fall transitions [1][5].

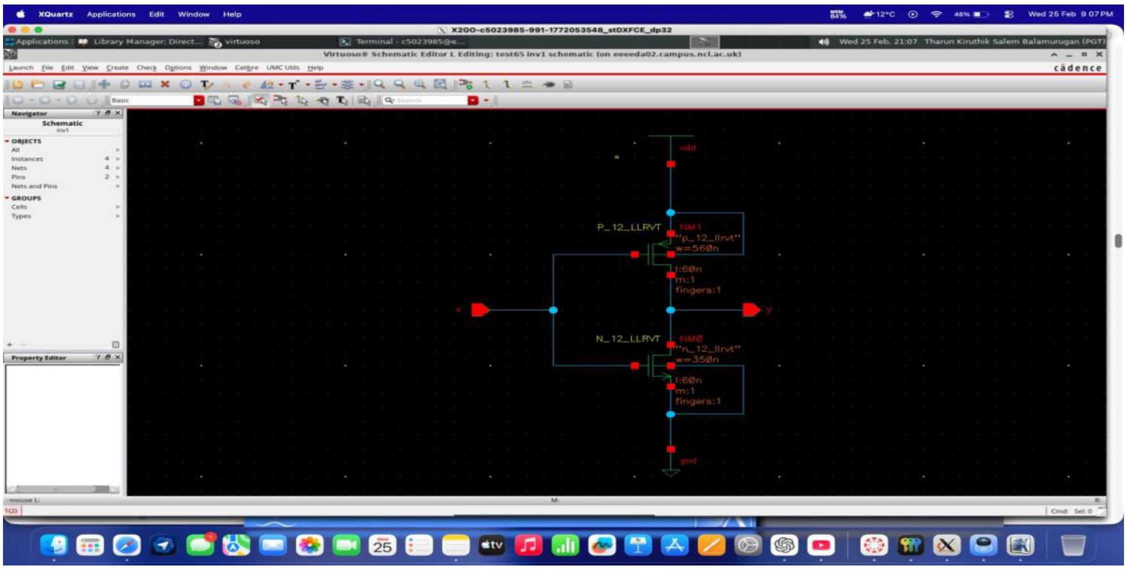

Fig. 1. Schematic of the CMOS inverter using P_12_LLRVT (PMOS) and N_12_LLRVT (NMOS) in UMC 65nm technology.

B. Transient Simulation and Delay Analysis

Transient simulations were performed using a pulse input switching between 0 V and 1 V. The measured propagation delay was t_pd ≈ 32 ps, consistent with first-order RC model predictions and confirming appropriate device sizing.

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Fig. 2. Transient response of the CMOS inverter showing input/output waveforms and measured delay of 32 ps.

C. Layout Implementation

The layout followed UMC 65 nm design rules with PMOS in the N-well and NMOS in the substrate. DRC and LVS verification confirmed fabrication compliance and electrical equivalence.

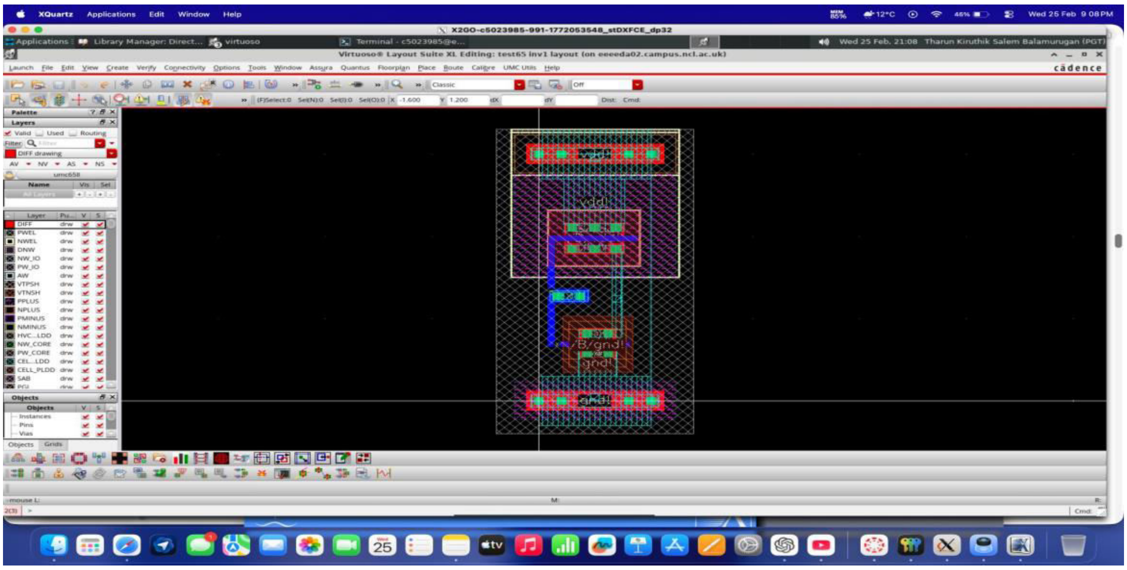

Fig. 3. Physical layout of the CMOS inverter in UMC 65nm technology.

IV. TRI-STATE INVERTER DESIGN AND ANALYSIS

A. Circuit Operation and Device Sizing

The tri-state inverter extends the standard CMOS inverter with enable-controlled series transistors, allowing a high-impedance (Hi-Z) output state. Transistor widths were doubled: PMOS W = 1.12 µm and NMOS W = 700 nm to compensate for increased series resistance where $R\_eq \approx R1 + R2$.

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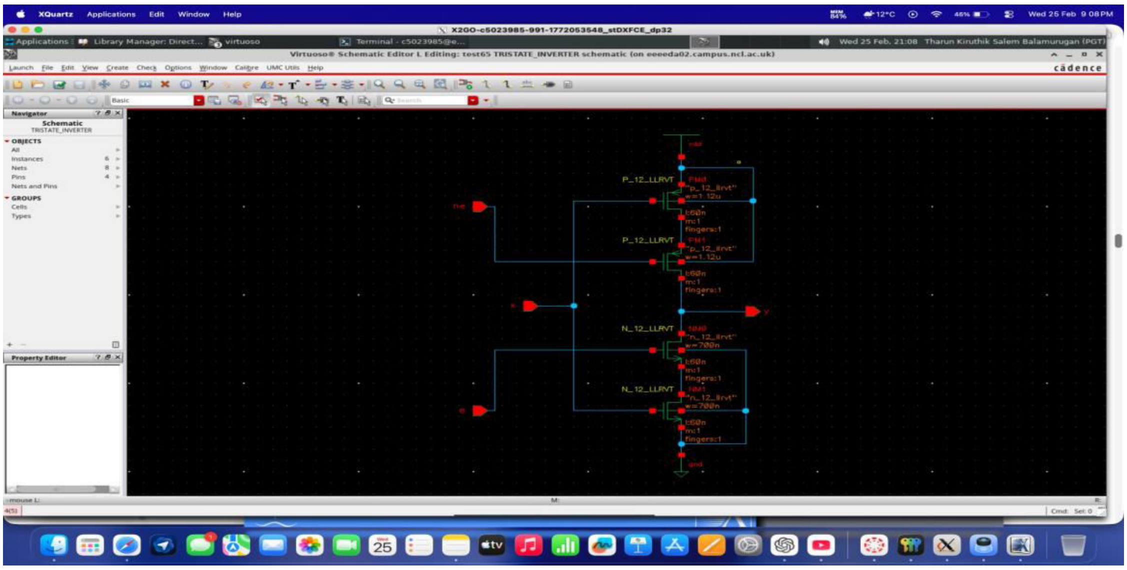

Fig. 4. Schematic of the tri-state inverter using series PMOS and NMOS gating transistors in UMC 65nm.

B. Simulation Results

The measured delay t_pd ≈ 52 ps represents a 62.5% increase over the standard inverter due to series resistance and additional internal node capacitances.

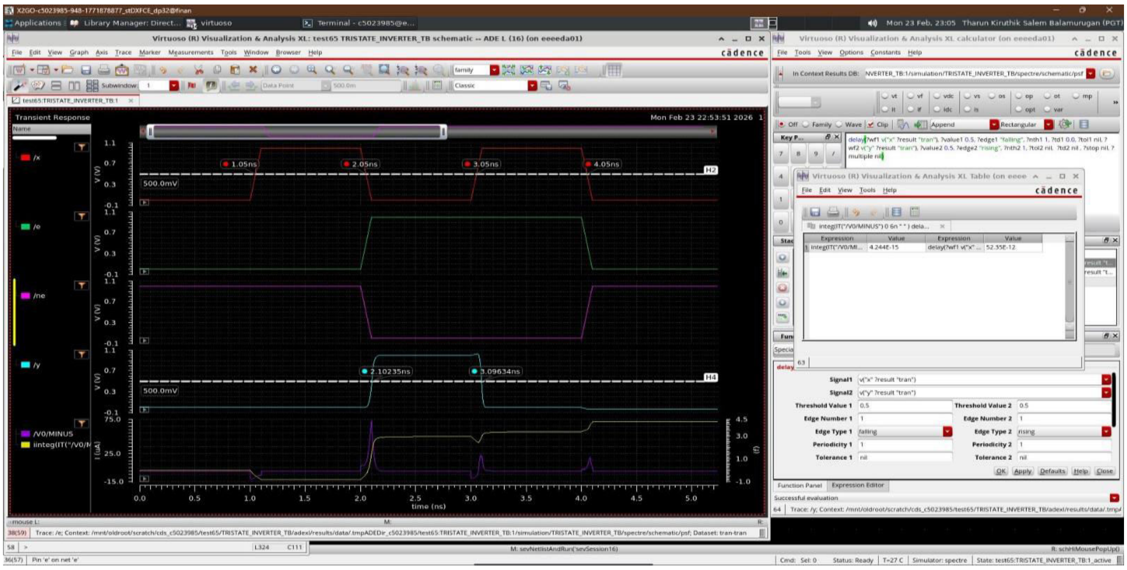

Fig. 5. Transient response of the tri-state inverter showing correct Hi-Z behaviour and t_pd ≈ 52 ps.

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C. Layout

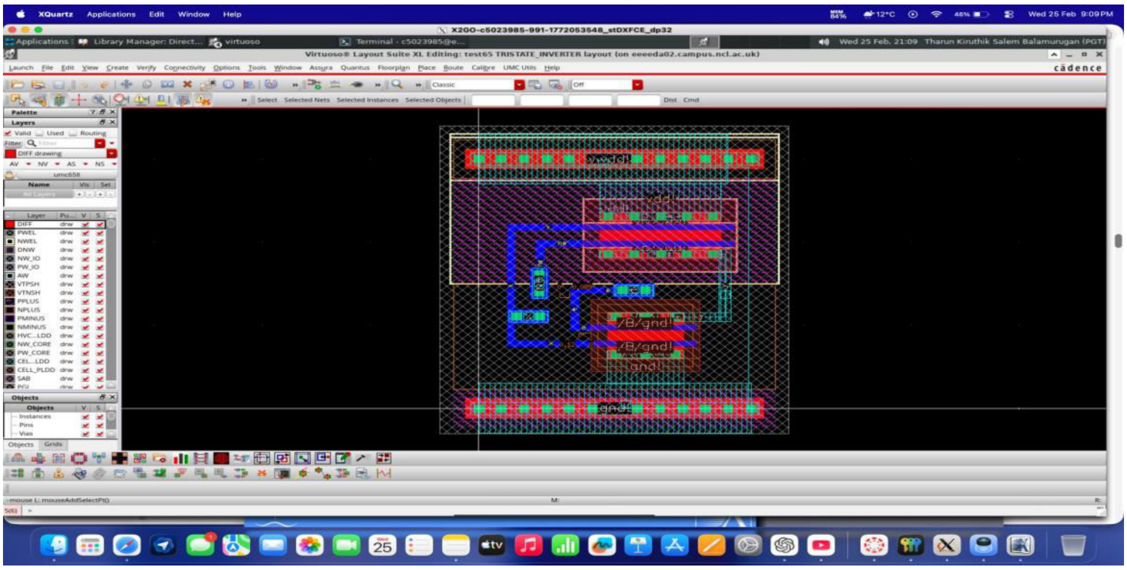

Fig. 6. Physical layout of the tri-state inverter in UMC 65nm technology.

TABLE I. Comparison Between CMOS Inverter and Tri-State Inverter

Parameter	CMOS Inverter	Tri-State Inverter
PMOS Width	560 nm	1.12 µm
NMOS Width	350 nm	700 nm
Transistor Count	2	4
Propagation Delay	≈32 ps	≈52 ps
Output States	0 / 1	0 / 1 / Hi-Z

V. D FLIP-FLOP DESIGN AND VALIDATION

A. Architecture and Design

The D flip-flop was implemented using a master-slave edge-triggered architecture built from the previously designed tri-state and CMOS inverters. The master latch is transparent when the clock is low; on the rising clock edge the slave propagates the stored value to output Q.

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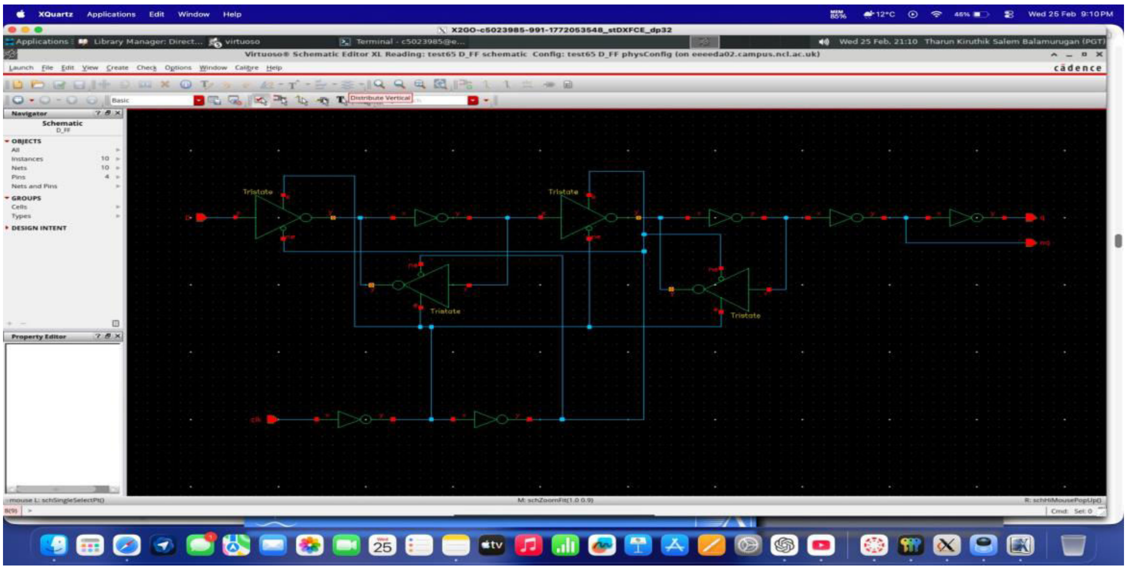

Fig. 7. Schematic of the edge-triggered D flip-flop using tri-state and CMOS inverters in UMC 65nm.

B. Functional Verification

Simulations confirmed correct edge-triggered behaviour: output Q changes only on the rising clock edge and remains stable between transitions.

Fig. 8. Transient response of the D flip-flop showing correct edge-triggered operation with clock, D, Q and NQ.

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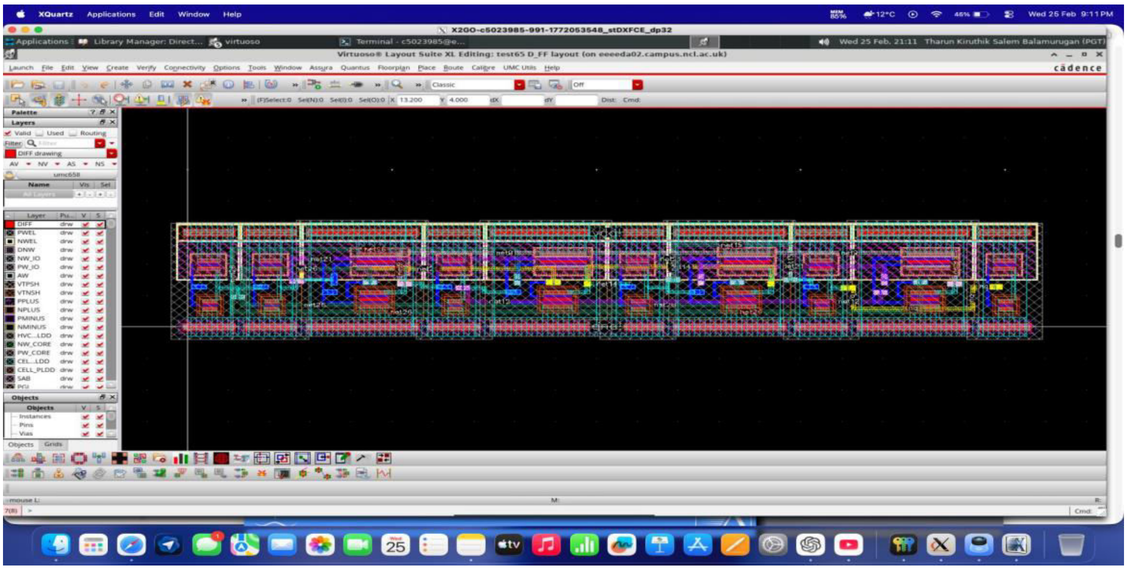

Fig. 9. Physical layout of the D flip-flop in UMC 65nm technology.

The correct operation of the D flip-flop hierarchically validates the inverter and tri-state inverter cells. The measured clock-to-Q delay was approximately t_cq ≈ 500 ps, consistent with the accumulated RC delay across cascaded master-slave stages.

VI. FAN-OUT ANALYSIS AND LOGICAL EFFORT

Fan-out analysis was performed by driving n identical inverter loads (n = 1, 2, 4, 8). Rising and falling propagation delays were measured at the 50% voltage threshold for each configuration.

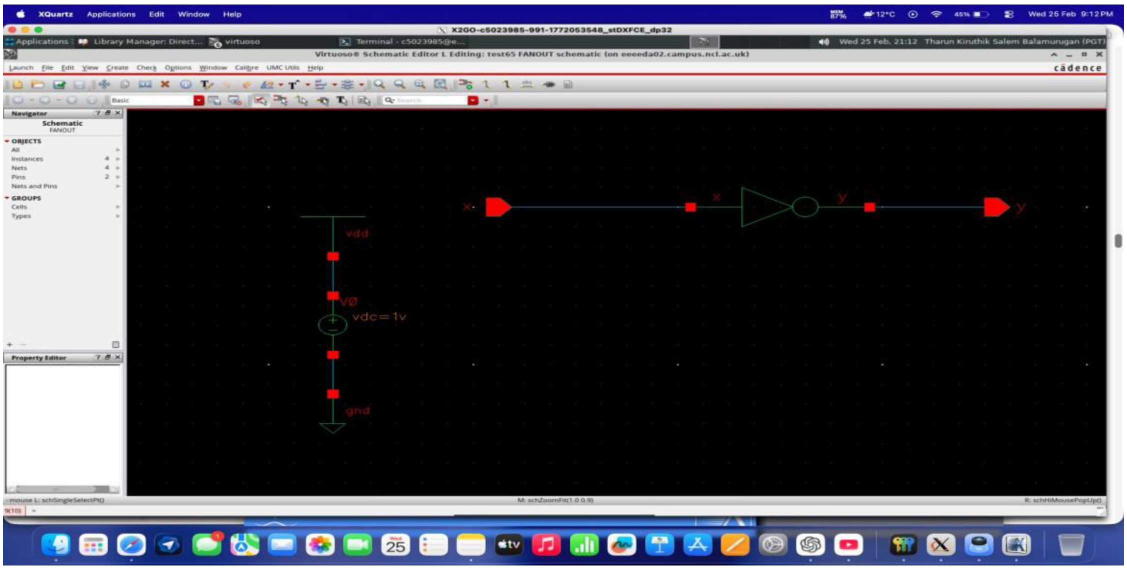

Fig. 10. FO1 configuration: one inverter driving one identical inverter load.

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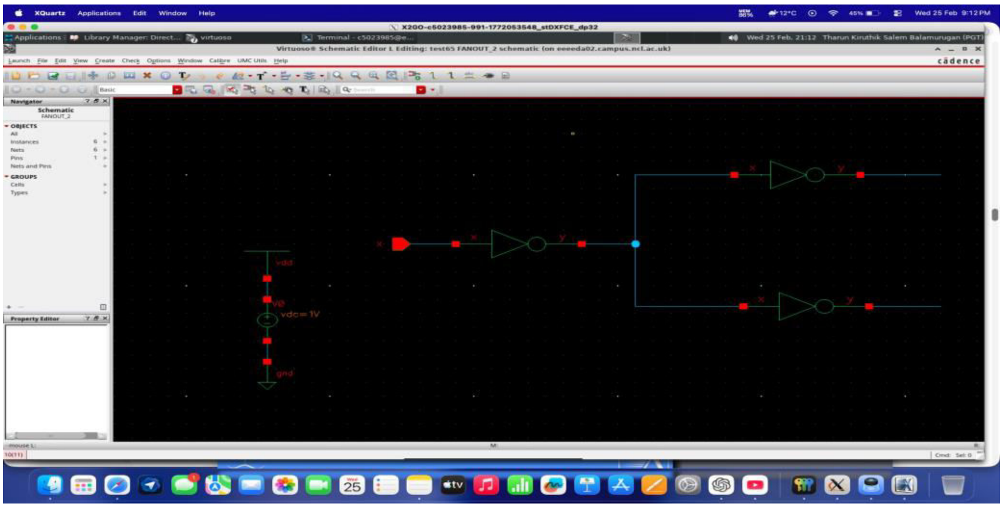

Fig. 11. FO2 configuration: one inverter driving two identical inverter loads.

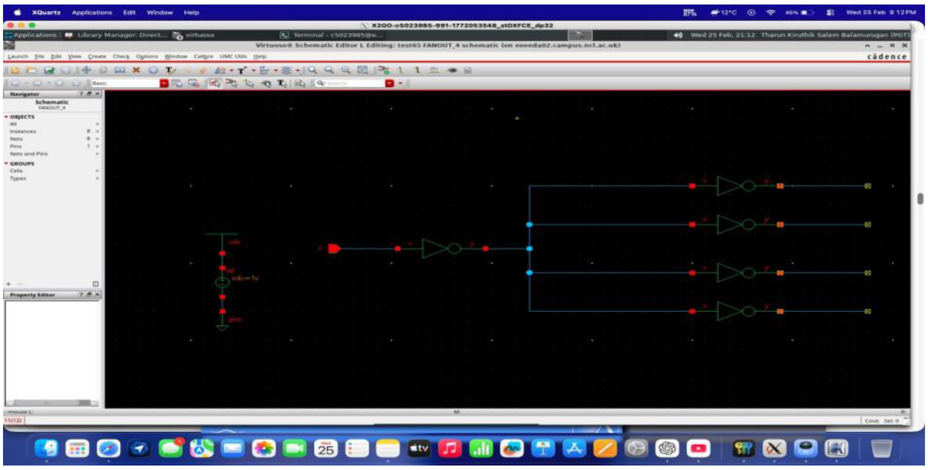

Fig. 12. FO4 configuration: one inverter driving four identical inverter loads.

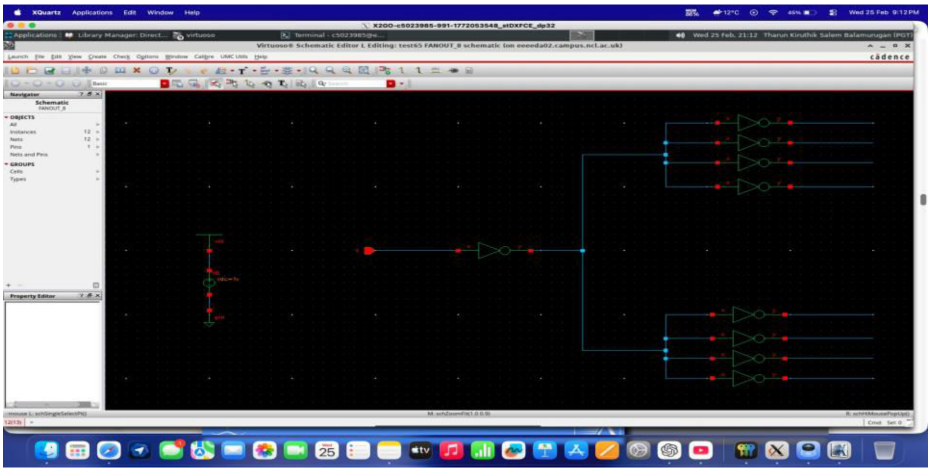

Fig. 13. FO8 configuration: one inverter driving eight identical inverter loads.

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Fig. 14. Rising propagation delay measurement for FO1: t_PLH = 21.05 ps.

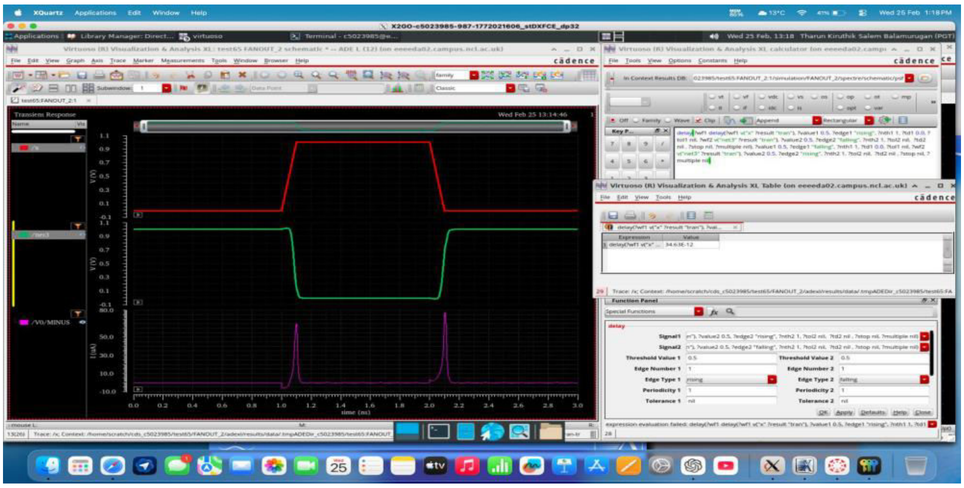

Fig. 15. Rising propagation delay measurement for FO2: t_PLH = 34.63 ps.

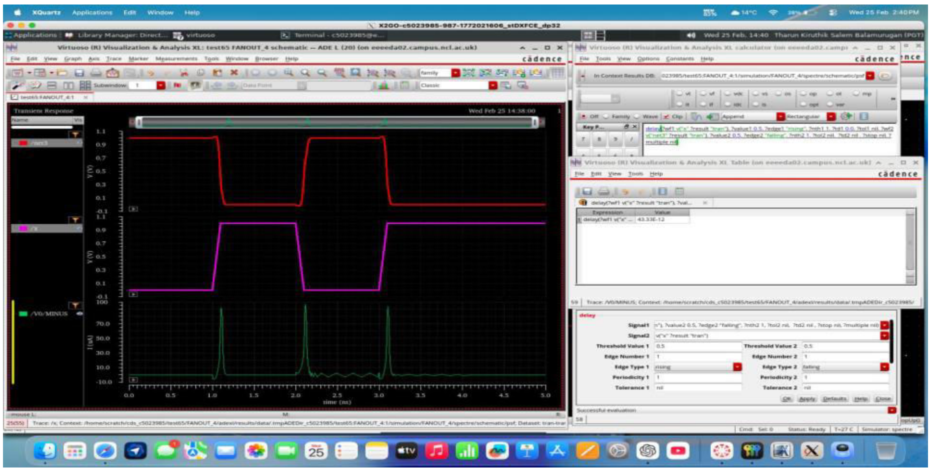

Fig. 16. Rising propagation delay measurement for FO4: t_PLH = 43.33 ps.

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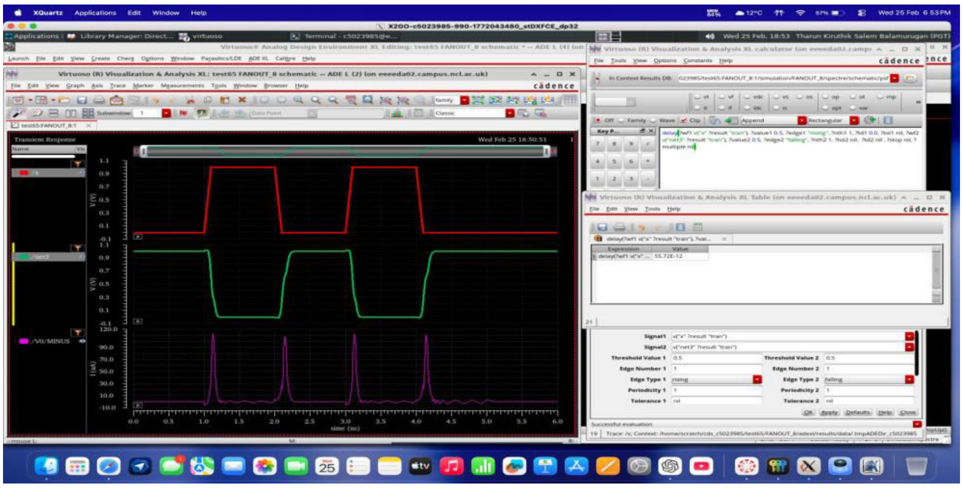

Fig. 17. Rising propagation delay measurement for FO8: t_PLH = 55.72 ps.

TABLE II. Fan-Out Delay Measurement Results

Config	t_PLH	t_PHL	t_pd (avg)	Ratio to FO1
FO1	21.05 ps	27.12 ps	24.09 ps	1.00×
FO2	34.63 ps	43.33 ps	39.00 ps	1.62×
FO4	43.33 ps	53.28 ps	48.31 ps	2.00×
FO8	55.72 ps	72.30 ps	64.01 ps	2.66×

Although load capacitance increases by 8× from FO1 to FO8, delay increases by only 2.66×, confirming the constant parasitic delay component predicted by logical effort theory.

VII. LONG WIRE DELAY EXPERIMENT

Two post-layout wire configurations were compared to quantify the impact of interconnect geometry on propagation delay. All measurements were performed post-PEX.

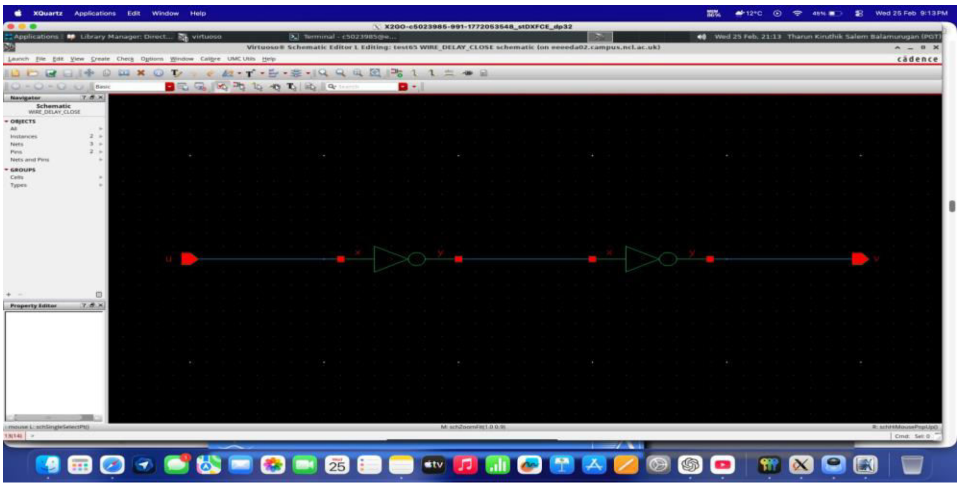

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Fig. 18. Close wire configuration schematic: driver inverter, short interconnect, receiver inverter.

Fig. 19. Transient response for close wire configuration: t_PLH = 60.53 ps.

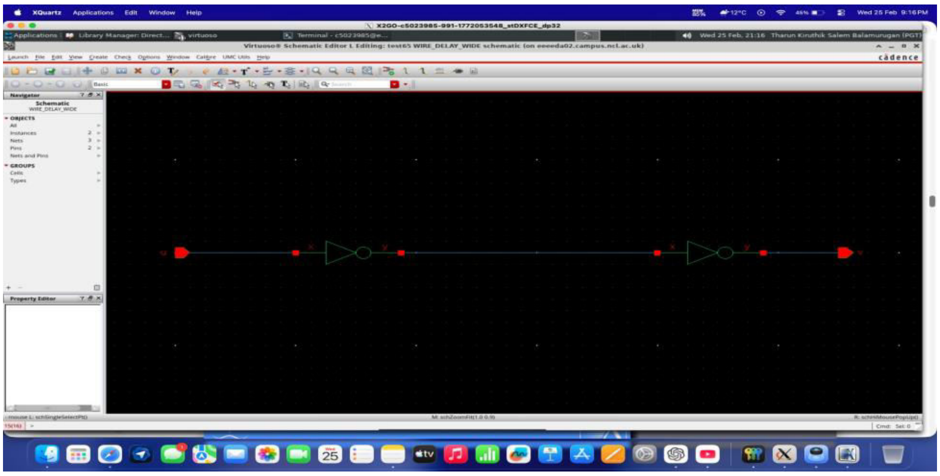

Fig. 20. Wide wire configuration schematic with increased wire width routing.

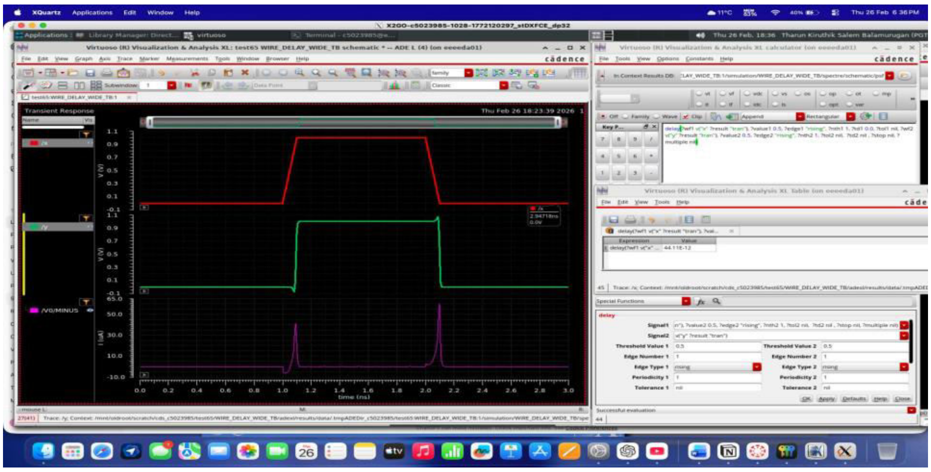

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Fig. 21. Transient response for wide wire configuration: t_PLH = 44.11 ps.

TABLE III. Wire Delay Comparison: Close vs Wide Configuration

Configuration	t_PLH	t_PHL	Avg Delay
Close	60.53 ps	68.08 ps	64.31 ps
Wide	44.11 ps	49.80 ps	46.96 ps

The wide configuration achieves a 27% reduction in delay. Increasing wire width reduces resistance ($R_w \propto 1/W$) while capacitance increases more gradually, so resistance reduction dominates.

VIII. PROPAGATION DELAY VS SUPPLY VOLTAGE

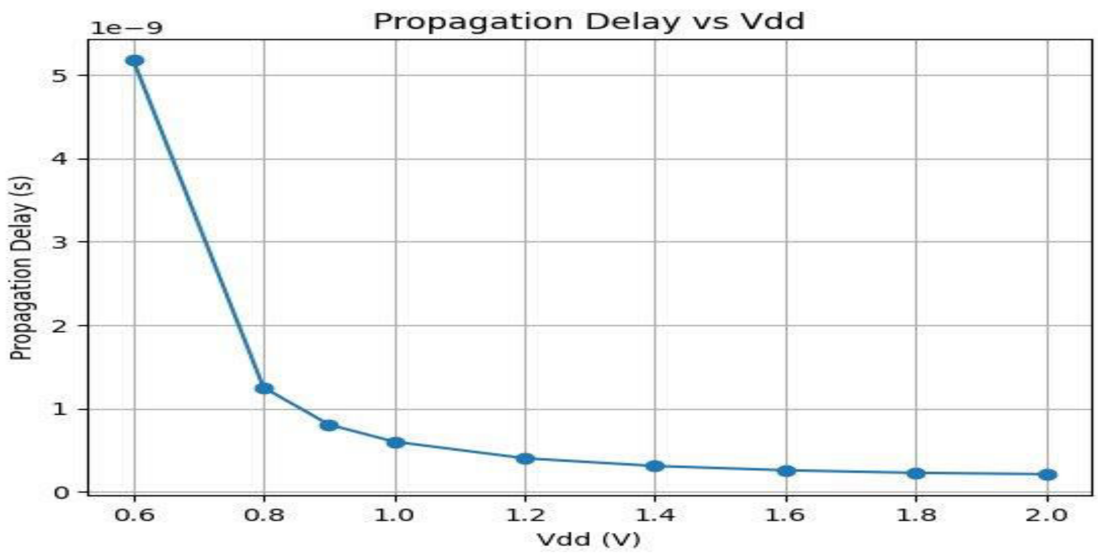

Fig. 22. Propagation delay versus supply voltage showing non-linear decrease as VDD increases.

TABLE IV. Propagation Delay vs Supply Voltage

VDD (V)	Rising Delay	Falling Delay
0.6	5.071 ns	5.289 ns
0.8	1.196 ns	1.231 ns
1.0	600.2 ps	605.6 ps
1.2	411.8 ps	397.1 ps
1.4	328.8 ps	294.3 ps
1.6	286.9 ps	233.0 ps
1.8	265.7 ps	191.8 ps
2.0	268.5 ps	159.3 ps

Delay decreases non-linearly as VDD increases, consistent with the alpha-power law model. The circuit becomes non-functional below 0.6 V due to insufficient overdrive voltage.

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IX. MINIMUM ENERGY POINT ANALYSIS

Total switching energy is: E_total = C_L × V_DD² + I_leak × V_DD × t_pd

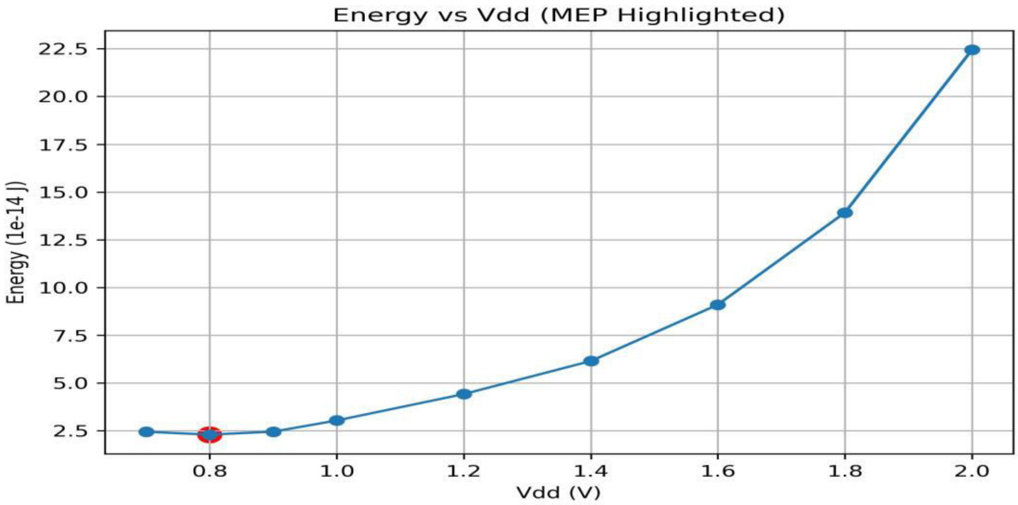

Fig. 23. Total energy per switching event vs supply voltage with MEP highlighted at 0.8 V.

The minimum energy point (MEP) occurs at approximately 0.8 V where total energy is ≈ 2.3×10^{-14} J. Below 0.8 V leakage energy dominates; above it, dynamic energy scales as V_DD². The MEP is particularly relevant for ultra-low-power IoT applications.

X. CONCLUSION

This paper presented the complete design, simulation, and timing analysis of CMOS digital circuits in UMC 65 nm technology. The CMOS inverter achieved t_pd ≈ 32 ps at 1 V, consistent with RC delay theory. The tri-state inverter showed a 62.5% delay increase due to series resistance. The D flip-flop validated the hierarchical correctness of the standard cells through correct edge-triggered operation.

Fan-out analysis confirmed that delay scales sub-linearly with load — only 2.66× for an 8× load increase — validating logical effort theory [6]. Wire delay experiments demonstrated a 27% delay reduction with wider interconnects, confirming that resistance dominates in 65 nm technology. Supply voltage scaling identified a minimum energy point at 0.8 V balancing dynamic and leakage energy.

Overall, the results confirm that accurate performance prediction in nanoscale CMOS requires both schematic-level analysis and post-layout parasitic extraction.

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